Design of Full Adder Using Subthreshold DTPT Logic

Kishore Sanapala and R.sakthivel

School of Electronics Engineering, VIT University, Vellore, Tamilnadu, India.

Abstract
As technology scaling has enabled small, design of digital circuits optimal for subthreshold region is becoming an active area for ultra low power applications.This paper presents the design of full adder using Subthreshold Dynamic Threshold Pass Transistor (Sub-DTPT) logic to achieve low power with acceptable performance. The simulations are carried out in cadence 90nm technology for V_{dd}=0.2V and 1.2V. From the simulations the Power Delay Product (PDP) of the proposed design is found to be extremely low in subthreshold region and is reduced by more than 80% when compared with the earlier reports. In strong inversion region the proposed adder is achieved more than 50% savings in delay when compared with the existing designs.
Keywords Full adder; PDP; Subthreshold region; Sub-DTPT logic; Ultra low power.

1 Introduction

Increase in the usage of modern portable battery operated devices such as wearable electronics, cellular phones, iPods and remote sensors are leading to the demand of ultra low power applications. From [**? ? ? ? ? ? ? ?**], it is noted that digital sub-threshold circuit design became the assured method for achieving the ultra-low power applications with acceptable performance. The sub-threshold voltage is basically the supply voltage (Vdd) less than the threshold voltage (Vth) of the transistor, circuits operating in this region consider the sub-threshold leakage current of the device for the necessary computations. Exponential reduction of power at the cost of reduced performance is the impact with the subthreshold region of operation. This impacts being positive, there has been interest for the digital computations which uses the subthreshold leakage current achieving in ultra low power consumptions in portable computing devices. The formerly parasitic sub-threshold leakage current is exploited by the operation in the sub-threshold or weak-inversion region, and this exploited leakage current is considered as the primary operation current[**?**]. These primary currents are considered to be much weaker comparatively to the standard strong-inversion currents; this will increase the time for charging or discharging the capacitive nodes which will limit the operation frequency of the circuit. In order to achieve ultra low power benefits, these leakage currents expected to drive the logic should be minimized in the device off state.

For an MOS transistor, when the gate to source voltage (V_{gs}) of the transistor

is biased under the threshold voltage (Vth), the subthreshold or weak inversion region of operation occurs. Vth is independent of the drain bias and the channel in case of a long channel device. The case differs when comes to submicron channel lengths and results in the effect of Drain Induced Barrier Lowering (DIBL)[**?**]. The drain current in the subthreshold region of operation is [**?**]

$$I_{DS} = I_0 e^{(V_{gs} - \eta V_{ds} - V_{th})/\eta V_T (1 - e^{\frac{-V_{ds}}{V_T}})} \tag{1}$$

where

$$I_0 = \mu_0 C_{0x} \frac{W}{L} (n-1) {V_{th}}^2 \tag{2}$$

and the parameters

V_T	Thermal voltage (KT/q = 26mV at 300^0K)
η	DIBL coefficient
n	subthreshold swing coefficient (n= $1 + C_{dep}/C_{Ox}$)
μ_0	zero bias mobility
C_{dep}	depletion capacitance
C_{Ox}	oxide capacitance
W	effective width of the channel
L	length of the channel
V_{ds}	drain to source voltage

As device behavior depends on many parameters, in this study of DTPT logic, bulk terminal voltage is the key variable choice. Varying the bulk terminal potential yields to further perceive into the device behavior to changes at the drain/ source and gate terminals. In the standard CMOS configuration the bulk of the NMOS is tied to the ground and the bulk of the PMOS is tied to the VDD for an inverter. It is found that the drain current increases, when the bulk potential raise above the ground and the VDD to below threshold for the NMOS and PMOS devices respectively[**?**]. One solution to increase/decrease subthreshold currents in on/off states is to use DTMOS configuration[**?**], where the bulk terminal is tied to its gate as shown in Fig.1 (a). Using DTMOS pass gate along with the augmented device tends to a new configuration as shown in Fig.1 (b) called DTPT[**?**].

This paper presents the full adder design using sub-DTPT logic for the first time in the literature. The remaining of this paper is organized as follows. Section 2 presents the brief description about existing full adder designs reviewed in comparison with the proposed design. The proposed sub-DTPT full adder design is described in section 3. Simulation results and performance parameters

of the comparisons made with respect to different adders are presented in section 4. Finally some conclusions are summarized in section 5.

2 Existing Full Adder Designs

The adder is the basic building block in many of the VLSI systems such as Digital Signal Processors (DSP) and microprocessors. Since adder is the core module in many of the arithmetic operations, enhancing the performance of this module would lead to enhance the overall system performance. Thus the design of full adder with lower PDP becomes the engineers interest for implementing the modern VLSI systems.

Number of adder circuits was designed using different logic styles and circuit techniques to reduce the power consumption and delay. The functionality of the adders compared in table1 is similar but differ in the design methodologies. Each logic style tends to favor one of performance aspects like power, delay, and area but at the expense of the other.

The different full adders are considered for performance comparison in conventional strong inversion region is discussed briefly in the following. The standard Complementary Metal Oxide Semiconductor (CMOS) adder is the more robust and most conventional design[**?** **?** **?**]. It is designed using the regular CMOS structure with pull up and pull down networks. Another conventional Complementary Pass Transistor Logic (CPL) with swing restoration logic is proposed in[**?** **?**]. It produces the complementary output of the many intermediate switching nodes. Voltage degradation is the main issue in the performance of CPL design. This was improved with the Transmission Gate Full Adder (TGFA) designs[**?** **?**]. Transmission Gate (TG) is constructed by connecting the PMOS and NMOS transistors in parallel. But the driving capability of the TGFA design is less when cascaded. This results in performance degradation.

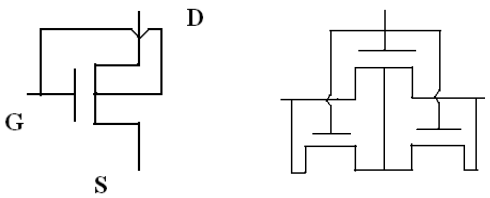
Later many hybrid logic styles which use more than one logic style in implementation are proposed. A 14 transistor hybrid adder was proposed in [**?** **?**] and Zhang et al. proposed Hybrid Pass logic with Static CMOS output drive (HSPC) adder [**?**]. In this logic the XOR and XNOR functions are generated concurrently by using pass transistors and implemented in CMOS module to produce full swing outputs. Chiou-kou Tung et al. proposed another hybrid FA core which uses the mirror type static CMOS logic to improve output driving capability[**?**]. Sumeer Goel et al. proposed a new hybrid adder which also targets high speed applications and is noise immune[**?**]. Mariano Aguirre et al. proposed a hybrid Double Pass transistor Logic (DPL) and Swing Restored CPL (SRCPL) full adders[**?**]. Multiplexing of the Boolean functions XNOR/XOR and OR/AND is used as internal logic style for implementing this full adder architecture.

The different full adders considered for performance comparison in Subthresh-

old region (for V_{dd}= 200mV) is discussed briefly in the following. Direct synthesis FA [**?**] is implemented based on Karnaugh map driven digital design and is realized using standard NAND and XOR gates. The other three different adders proposed in [**?**] are Min3 stacked FA, Min3 mirrored FA, and Min3 IJCNN FA. These three adders are based on the Stacked Minority 3 element[**?**], Mirror Minority 3 element[**?**], CMOS inverter and dynamically reconfigurable IJCNN element[**?** **?**]. Min3 mirrored adder is suitable only for low performance applications because of its large power dissipation. Min3 stacked and IJCNN adder architectures are applicable for low noise margin systems.

3 Proposed Sub-DTPT Full Adder

Many circuit techniques are introduced to operate the digital circuit in subthreshold region to meet the ultra low power requirement. In all the subthreshold digital circuits, power supply less than the threshold voltage of the transistors is used to power the circuit. In the subthreshold region, there is no conducting inversion channels, so therefore, the transistors behave in different manner as compared to when they are operated in a strong inversion region. Therefore, there will be a change in the circuit properties, such as noise margin, tolerance to temperature and process variations. Thus there are noted favorable changes, such as increased transconductance gain, near-ideal static noise margin, sensitivity of subthreshold circuit to power supply, temperature and process variations [**?** **?**]. This increase in the sensitivity may lead to improper functioning of the subthreshold circuits. Thus to make sure proper functioning of the subthreshold circuits, moalemi et al.[**?**] and Lindert et al.[**?**] proposed a logic family called sub-DTPT logic which gives lesser PDP when compared other subthreshold logic families reviewed in [**?**].



(a) (b)

Fig. 1 (a) Standard DTMOS (b) DTMOS with pass gate

Sub-DTPT logic uses the dynamic threshold transistors whose gates are tied to the substrates. To mitigate the drop problem, restoration has been commonly used; this will assist the pass-gate pull-up at the output. A new idea in pass-gate

logic is to use Dynamic Threshold MOS (DTMOS)[**?**] for restoration, but the combination of the two will help scale the voltage even further. To provide a new symmetric design to the circuit, augmented circuit styles need to be customized for pass-gate logic, which makes it to add a secondary auxiliary device. The DTMOS pass gate with the augmented device is known to be Sub-DTPT and is shown in Fig.1(b) and the standard DTMOS is shown in Fig.1(a).

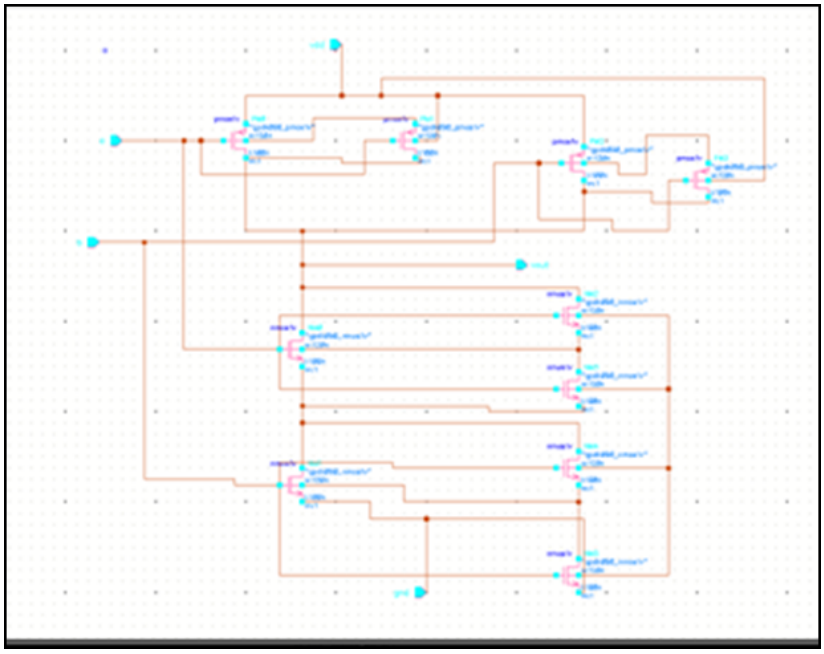


Fig. 2 Subthreshold DTPT NAND gate

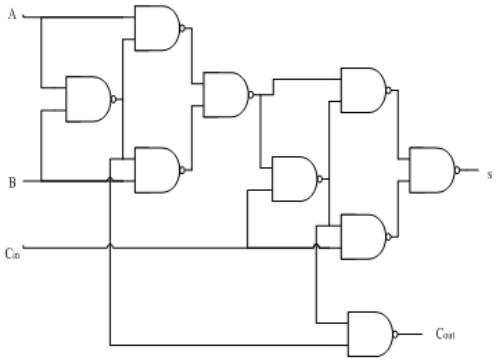


Fig. 3 Full Adder using Sub-DTPT NAND gates

The design of NAND gate using the sub-DTPT logic is as shown in the Fig.2.

The combinational circuit full adder is designed in sub-DTPT logic, since the full adders are the basic digital blocks in many of the arithmetic units. Because of the universal characteristics, of NAND/NOR gates, engineers prefer these universal gates in the design of combinational digital circuits. In the proposed design, the full adder is realized using only NAND gates. Since NOR gate has more delay because of the series stack of PMOS transistors in series. The full adder using subthreshold DTPT NAND gate is shown in Fig.3.

4 Results and Discussion

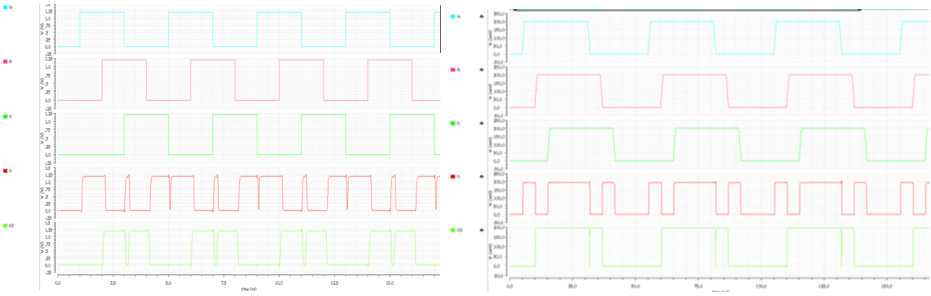
The proposed sub-DTPT full adder is simulated using cadence virtuoso tool in 90nm technology for the supply voltages of 1.2v (strong inversion region) and 200mV (Subthreshold region). The obtained simulation waveforms are shown in Fig.4. The performance parameters power, delay and Power Delay Product (PDP) are measured for the proposed design and also compared with the existing designs. The comparisons for the proposed adder with different existing full adders in conventional strong inversion region and subthreshold region are shown in Table 1 and Table 2 respectively.

The longest delay is considered as the cell delay which is obtained by considering the 50% of the input voltage swing to the 50% of output voltage swing. The average power is measured using the predefined calculator functions available in the cadence virtuoso tool.

From the comparisons in the table 1, it is noted that in strong inversion region, the proposed design achieved major s avings in terms of delay and is 36.25% less than the FA-SRPL, 58.26% less than the FA-DPL designs proposed in [**?**], approximate 25% less than the Sumeer Goel design[**?**] and Chiou-kou Tung

Table 1 Results of the simulations for full adders in 90nm technology with V_{dd}=1.2V

Design	Reference	Power(μW)	Delay(ns)	PDP(fJ)
C-CMOS	[**?** **?**]	1.5799	0.1274	0.20127
CPL	[**?** **?** **?**]	1.7683	0.0791	0.13987
TGFA(16T)	[**?** **?**]	1.7459	0.3258	0.5688
TGFA(20T)	[**?** **?**]	1.7796	0.2348	0.41785
14T HYBRID	[**?** **?**]	3.3328	0.3377	1.1254
HSPC-HYBRID	[**?**]	1.576	0.2301	0.3626
Mirror type-HYBRID	[**?** **?**]	7.707	0.1406	1.0836
FA-HYB	[**?**]	6.21	0.143	0.888
FA-DPL	[**?**]	7.34	0.254	1.864
FA-SRPL	[**?**]	7.4	0.167	1.235
PROPOSED	[Present]	12.3704	0.10646	1.31695



(a) (b)

Fig. 4 (a) Simulation response of the proposed full adder design for V_{DD}=1.2V; (b) Simulation response of the proposed full adder design for V_{DD}=0.2V.

et al.[**?**], more than 53% less than the hybrid HSPC adder design and 20T TGFA design, more than 65% savings than the Vesterback et al.[**?**] adder and 16T TGFA and also 16.4% less than the conventional CMOS adder. It is also noted that the power delay product (PDP) of the proposed adder is 29.2% less than the FA-DPL design.

Table 2 Results of the simulations for full adders in 90nm technology with V_{dd}=0.2V

Design	Reference	Power(pW)	Delay(ns)	PDP(aJ)
Direct Synthesis	[**?** **?**]	854.1	263.5	225.3
C-CMOS	[**?** **?**]	931.6	162.4	151.3
Min3-stacked	[**?** **?**]	191.8	4767.7	914.5
Min3-mirrored	[**?** **?**]	1160	159.1	184.6
Min3-IJCNN	[**?** **?**]	5206	173.7	904.1
PROPOSED	[Present]	2293	69.25	158.79

From the comparisons in Table2 it is noted that proposed adder has achieved major savings in terms of PDP and is more than 82% lesser than the min3-IJCNN and min3 stacked adder designs, 29.5% lesser than the direct synthesis adder design and also 13.98% lesser than the min3 mirrored adder design.

From the above result analysis, it is observed that the delay of the sub-DTPT design is extremely low but the power is found to be very large. This increase in power is due to the excessive gate current caused by forward biasing the source body junctions.

5 Conclusions

In this paper, the design of full adder using Dynamic Threshold Pass Transistor logic is presented. The simulations are done using cadence virtuoso 90nm

technology for supply voltages of 1.2V and 0.2V. At 1.2V, the results of the proposed design are compared with many logic styles like conventional CMOS, CPL, TGFA, Hybrid, SRPL and DPL. At 0.2V, the results of the proposed logic is compared with different logic designs proposed earlier like standard CMOS and Min-3 based adders. From the simulations, it is found that in subthreshold region of operation the proposed design achieves major savings in the PDP compared with the previous reports. The proposed logic is useful in the implementation of the chip which overcomes the issues like power, delay, DIBL, and process sensitivity. Further improvements can be done for the proposed design in reducing the area overhead.

References

[1] K.Roy and H.Soeleman (1999), "Ultra low power Subthreshold digital logic circuits", *proc. IEEE conf. Low power electronics and design*, pp. 94-96.

[2] A.Chandrakasan and R.Broderson (1995), *Low Power Digital CMOS Design*, Springer, Boston.

[3] A.Wang, B.H.Calhoun and A.chandrakasan (2006), *Subthreshold Design For Ultra Low Power Systems*, Springer.

[4] J.M.Rabaey and M.Pedran (1996), *Low Power Design Methodologies*. Springer, Boston.

[5] Nyathi and Jabulani (2006), "Logic circuits operating in Subthreshold voltages", *Proc. IEEE conf. Low Power Electronics and Design*, pp. 131-134.

[6] J.Kao, S.Narendra and A.Chandrakasan (2006), "Subthreshold leakage modeling and reduction techniques", *Proc. IEEE conf. Low power Electronics and Design*, pp. 131-134.

[7] K.Roy and H.Soeleman (2001), "Robust Subthreshold logic for ultra low power operation", *IEEE Trans. Circuits and Systems*, Vol. 9, pp. 90-99.

[8] J.M.Rabaey, A.Chandrakasan and B.Nikolic (2003), *Digital Integrated Circuits-A Design Perspective (*2^{nd}*ed.)*, Pearson eduction.

[9] N.Lindert, T.Sugii and S.Tang et al. (1999), "Dynamic threshold pass transistor logic for improved delay at lower supply voltages", *IEEE Journal of Solid State Circuits*, Vol.34, pp. 85-89.

[10] Zhang.M, J.Gu and CH.Chang (2003), "A novel hybrid pass logic with static CMOS output drive full adder cell", *Proc. Int.Symp Circuits and Systems*, pp. 317-320.

[11] N.H.Weste and David Harris (2004), *CMOS VLSI Design- A Circuits and Systems Perspective (3rded.)*, Addison Wesley.

[12] Issam.S, Khater.A and Bellaouar.A et al.(1996), "Circuit techniques for C-MOS low power, high performance multipliers", *IEEE Journal of Solid State Circuits*, Vol.31, pp. 1535-1544.

[13] A.M. Shams, Darwish.T and M.Bayourmi (2002), "Performance analysis of 1-bit low power full adder cells", *IEEE Trans. Very Large Scale Integration Systems*, Vol. 10, pp. 20-29.

[14] N.Jhuang and H.Wu. (1992), "A new design of the CMOS full adder", *IEEE Journal of solid state circuits*, Vol.27, pp. 840-844.

[15] K.Navi, R.F.Mirzaee and M.H.Moyaeri at al. (2007), "A novel low power full adder cell with new technique in designing logical gates based on static CMOS inverter", *Micro electronics.J.*, Elsevier, Vol. 38, No. 1, pp. 130-139.

[16] K.Navi, V.Foroutan and M.R.Azghadi at al. (2009), "A novel low power full adder cell with new technique in designing logical gates based on static CMOS inverter", *Micro Electronics.J.*, Elsevier, Vol. 40, pp. 1441-1448, Aug. 2009.

[17] C.K.Tung, S.H.Sheih and Y.C.Hung. (2007), "A low power hybrid CMOS full adder for embedded system", *Proc. IEEE conf. Design Diagnostic. Electron. Circuits Syst.*,Vol.13, pp. 1-4.

[18] S.Goel, A.Kumar and M.A.Bayoumi (2006), "Design of robust, energy efficient, full adders for deep sub-micrometer design using hybrid CMOS logic style", *IEEE Trans. Very Large Scale Integration Systems*, Vol. 14, pp. 1309-1321.

[19] Mariano Agurrie-Hernandez and M.L.Aranda (2011), "CMOS full adders for energy efficient arithmetic applications" , *IEEE Trans. Very Large Scale Integration Systems*, Vol. 19, pp. 718-721.

[20] Kristian.Aunet.S. (2006), "Six subthreshold full adder cells characterized in 90nm CMOS technology", *Proc. IEEE conf. Design Diagnostic. Electron. Circuits Syst.*, Vol.13, pp. 25-30.

[21] Aunet.S and Y.Berg (2005), "Three sub-Fj power delay product subthreshold CMOS gates", *IFIP VLSI Soc*, Perth, Australia.

[22] Aunet.S, Oelmann.B and Abdalla.S et al. (2004), "Reconfigurable Subthreshold CMOS perceptron", *International Joint Conference on Neural Networks, IJCNN*, Budapest, Hungary, vol.13., pp. 25-29.

[23] Aunet.S, Norweigan and Kretselement (2003), Patent application, no.20035537, Leiv Eiriksson Nyskapning, Trondheim, Norway.

[24] B.H.Calhoun, Al.Wang and A.Chandrakasan (2005), "Modeling and sizing for minimum energy operation in subthreshold circuits", *IEEE Journal of Solid State Circuits*, Vol.40, pp.1778-1786.

[25] Vahid.M and Ali A.K. (2007), "Subthrelod pass transistor logic for ultra low power operation", *IEEE Computer Society Annual Symposim on VLSI.*, pp.490-491.

[26] Ramesh.V, S.Dasgupta and R.P.Agarwal (2009), "Device and circuit design challenges in the digital subthreshold region for ultra low power applications", *Hindawi publishing corporation VLSI design.*

[27] Jiangmin.Gu and CH.chang (2003), "Ultra low voltage, low power 4-2 compressor for high speed multiplications", *Proc. IEEE International Symposium on Circuits and Systems*, pp. 321-324.

[28] Alioto.M, Di cataldo.G and Palumbo.G. (2007), "Mixed full adder topologies for high performance low power arithmetic circuits", *Micro Electronics.J.*, Elsevier, Vol. 38, No. 1, pp. 130-139.

[29] C.H.Chang, J.M.Gu and Zhang.M. (2005), "A review of 0.18μm Full adder performances for tree structured arithmetic circuits", *IEEE Trans. Very Large Scale Integration Systems*, Vol. 13, pp. 686-695.

[30] P.Bhattacharyya, Bijoy.K and S.Ghosh et al (2014), "Performance analysis of a low power high speed hybrid 1-bit full addert circuit", *IEEE Trans. Very Large Scale Integration Systems*, Vol. 23, pp. 2001-2008.

Corresponding author

Kishore Sanapala can be contacted at: kishorelendi@gmail.com