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# Leakage Power Reduction in Read and Write Enhanced Macro Memory Circuit Design Using Transistor Stacking and Reversible Approach

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**Abstract**: Power dissipation is one of the on-demand problems of low power Very large-scale integration (VLSI) circuit design and it is related with threshold voltage. Generally, the subthreshold leakage current and the leakage power dissipation are increased while reducing the threshold voltage. The overall performance of the total power dissipation is completely depending on this leakage power dissipation. This leakage power causes the components that are functioned by battery for a long period washed-out rapidly. In this paper, a new read decoupled and write enhanced macro memory design is proposed using transistor stacking and reversible logic to reduce the leakage power. For the reduction of power consumption of Static Random Access Memory (SRAM) that are placed in System on Chips (SoCs), the proposed model includes three features: a reversible cross coupled stacked inverter with Transmission gate is adopted in SRAM cell to reduce the leakage power, a reversible differential power generator is adopted to improve the write ability of the design with less power and a read burst mode is used to reduce the read energy while reading consecutive addresses**.** Furthermore, a reversible logic is applied in all the peripheral circuits, which gives additional level of confidence in terms of leakage power. The simulation results show that the leakage power of the proposed macro memory design is reduced to $2.22nW$ at 0.6V supply, which is $4.32nW$ less than that of the conventional macro design. Furthermore, the write and read power consumption of the proposed macro design is reduced by 57% and 66% as compared to conventional one at a supply voltage of 0.6 V.

***Keywords***: macro memory design, SRAM, leakage power, reversible logic, Toffoli gate, reversible differential power generator

## 1. INTRODUCTION

Generally, the portable and battery-operated devices often embed System-on-chips (SoCs). Static Random-Access Memory (SRAM) occupies most of the chip area in SoC [1-2]. Furthermore, the progression of low power neural network accelerators in different applications has made a strong request for power-efficient SRAM design [3-4]. Similarly, the battery-less SoCs, needs three different types of memories: a “hold mostly” memory to save critical information for the longest possible time when energy is scarce, a “read-mostly” memory to hold the program instructions that run on the SoC, and a “read-write” memory to save the data gathered. For the SoCs to support all three types of memories and still operate on harvested energy, the power and energy consumption of these memories must be kept at a minimum. In the last few decades, scaling is utilized for accomplishing highly standard CMOS devices. This scaling process is used to reduce the delay and area of the systems. However, the shrinking of device dimensions rises the leakage current and power as well. In

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general, SRAM cells contains nanoscale components while minimizing the size of CMOS technology. As a result of this, the vulnerability of SRAM to soft errors is increased because of their more integrated density and lower supply voltage [5-6].

SRAM requires to be more vigorous, cost-effective, and consume less power when operating well at low supply voltages. Furthermore, the data storing ability of the reading and writing processes affects the SRAM structure [7-8]. Therefore, it is necessary to minimize the leakage power dissipation and improve the stability of SRAMs. The traditional SRAM designs are susceptible to regular read upsets due to their worsened read static noise margin (RSNM). The traditional SRAM design uses same port for both read and write operation. This degrades the stability of the design while the voltage at the 'zero' storage node surpasses the NMOS transistor's threshold voltage [9]. For improving the stability as well as rapidity of dual port memories, different write and read bit lines are required.

The dependency of temperature is the main reason for leakage power dissipation on CMOS circuits. Recently, several leakage power reduction methods have been designed specifically for SRAM structures. They are sleep transistor approach, Sleepy stacking method, power gating method and LECTOR approach. These approaches stack leakage path with the help of OFF transistors [10-12]. The stacking transistor aims to develop power efficient SRAM structure with simpler design construction. This approach minimizes the leakage noise current at the time of reading process. The stacking method serially connects the transistors for avoiding the leakage current [13]. The sleepy transistor approach uses additional control circuity to generate sleep signals. It introduces additional area and power penalties in the SRAM design. The effectiveness of LECTOR approach is lesser than those of the complete OFF transistor method [14].

Power gating method is also named as low power design methodology. This approach adds additional header and footer transistors for isolating the supply and ground terminals when it is in inactive condition [15]. This approach uses several sleep transistors and hence it significantly increases the area usage. Furthermore, power gating method generates more voltage oscillations in the power/ground rail while changing the mode from power gating mode to active mode. This voltage oscillations are named as power/ground bouncing noise and it generates undesirable changeovers in the nearby non-power gated regions.

When the supply voltage (VDD) is decreased the dynamic or active power will be reduced drastically. Hence, the power-efficiency in SRAM cell has been achieved by downscaling the supply voltage [16]. This downscaling of supply voltage helps to reduce both static and dynamic power efficiently. However, this down sampled supply voltage is limited due to the inconsistency among the read and write necessities and direct-read-access strategy. The read line is separated from the primary cell of the single-ended SRAM design to optimize the enabling power supply of the read and write processes self-sufficiently. Also, the half-select disturbance suffers majority of the SRAM cell designs. Hence, the SRAM design structure needs to be improved for the minimization of leakage power as well as stability.

Furthermore, most of the available leakage reduction techniques can only moderate the circuit leakage power in standby mode. So, more efficient active leakage power reduction techniques are still essential to keep the leakage power and this motivate us to develop an enhanced technique for macro memory circuit design. The design of transistor stacking reversible logic circuits is a trending concept to achieve zero power dissipation. Series connected transistors or the stacking technique are utilized to minimize the subthreshold leakage currents. Similarly, the reversible data handing methods decreases the heat dissipation through the calculations, which preserves the energy and data without dissipating it into heat. This paper mainly aims to develop an efficient leakage power reduction approach for memory circuit. The main contributions of the proposed macro memory design are summarized as follows:

- To combine the benefits of both transistors stacking and reversible logic circuits in the macro SRAM design for the reduction of leakage power.
- To adopt the SRAM cell design using reversible cross coupled stacked inverter with Transmission gate for reducing the leakage power in the discharging path of SRAM cell.
- To enhance the write stability of SRAM cell by proposing a new reversible differential power generator write assist circuitry. This circuit is used to enhance the Write Static Noise Margin (WSNM) of the SRAM without compensating the power dissipation.
- To introduce a new feature of read burst operation (RBO) in the SRAM macro design, which reduced the read power whenever the successive addresses must be read for further processes. This feature will be more useful for "frequently read" applications such as image and video processing.
- To introduce an additional level of confidence in terms of stability, area and leakage/static power by developing a reversible logic based peripheral circuits in the macro SRAM design.

Rest of the paper is organized as follows: Section 2 reviews recent related works on SRAM design. Section 3 provides detailed description about the proposed macro memory design. Section 4 validates the simulation results of the proposed method. Finally, the paper is concluded in Section 5.

## 2. RELATED WORKS

Some of the recent related works are summarized as follows:

Saranya et al [17] used power gating method to reduce the power consumption of SRAM design. This approach ignored the straight link between the supply and ground by producing a virtual link between them. Pal et al [18] proposed a low power single ended SRAM cell that supported the concept of bit-interleaving for healthcare application. The primary cell of this SRAM design contained cross coupled inverters and feedback cutting mechanism to improve write stability. This structure exhibited a slightly lengthier write time due to the utilization of feedback cutting approach. Kumar et al [19] proposed a triple-threshold method for optimizing the power in SRAM design that improved the system stability in lesser CMOS technologies. These multiple threshold transistors played an important role in leakage power minimization task. But the sensitivity of leakage current developed from different transistors were high on process variants.

Kumar et al [20] performed a comparative study on the design constraints of different SRAM design such as such as sleepy keeper, stacked keeper with body bias, and leakage feedback approach for leakage power reduction. Among that, the SRAM cell that used stack transistor in the read trail reduced the read power dissipation. Satyaraj et al [21] compared the performance of different leakage power reduction methodologies such as sleepy stack approach, sleepy keeper approach, dual stack power gating and Dual controlled stacking (DCS) on SRAM memory. Gavaskar et al [22] used Hybrid VLSI methods to reduce and improve the Leakage and speed of the SRAM Cell respectively. Initially, they described the schematics of the conventional leakage power reduction methods such as GALEOR [23], LECTOR [23], Multi-threshold CMOS (MTCMOS) [24], Drain Gating [25], Sleepy Keeper [26], Leakage control NMOS transistor (LCNT), dynamic threshold MOS (DTMOS) and MTCMOS Ground Gated approach [27].

To tackle the issues of these methods, two or more leakage power reduction methods were combined to form hybrid models, for example Sleepy Keeper and Drain Gating approach, Drain Gating approach and Helper Transistors, upper self-controllable voltage level (USVL) and Trimode MTCMOS Ground Gated approach, lower self-controllable voltage level (LSVL) and Trimode MTCMOS Power Gated method. Among them, the hybrid TRIMODE MTCMOS power and ground gated method provided good performance in terms of power, delay and area. However, the size and cost of this SRAM cell is high as

compared to DRAM cells. Eslami et al [28] presented a new SRAM design that improved the stability of read, write, and hold processes without degrading the performance in terms of leakage power. The data has been floated temporarily at lower voltage to increase the capability of writing process. At the same time, the data storage node has been separated from the read bit line with the help of a transistor to maintain the read stability as same as that of the hold state. This structure connected an additional p-type access transistor for mitigating the write '1' problems of single ended SRAM design.

Sharma et al [29] introduced a data-dependent-power-supply approach to reduce the leakage power and improve the read/write stability for a 11T SRAM cell. This cell consumed picowatt range static power and enhanced the write static noise margin (WSNM) considerably. Furthermore, a read decoupling has been used with column-based read buffer for improving the read stability. The use of a data dependent power supply approach helped to avoid the requirement of an exclusive power supply, so that the leakage power of the SRAM cell has been reduced considerably. Wang et al [30] introduced a novel leakage minimization approach by splitting the array cell into two voltage regions. These regions were connected serially between the supply and ground for the straight generation of subthreshold holding voltage from the nominal supply. Here, the Zigzag cell arrangement has been selected with optimal transistor for balancing the hold stability, leakage, and area density.

Lorenzo et al [31] used a power gating transistor and transmission gate in SRAM design to reduce the leakage power and improve the reliability of writing process. The capabilities of read and write processes have been improved by separating the read and write path. Moreover, it eliminated the irrelevant bit-line discharging using a row dependant virtual ground signal. Peng et al [32] proposed a new 12T SRAM design by incorporating reverse bias current eliminating feature and read decoupling strategy. As a result of this, the read and hold static noise margin have been increased. Alternatively, Sachdeva et al [33] introduced a 12T SRAM cell on the bases of Schmitt trigger. Here, the properties of an inverter design have been improves using Schmitt trigger inverter.

This analysis shows that the leakage power dissipation and data stability are considered as the two main concerns while developing SRAM memory cell. To tackle the issues of traditional designs of SRAM, several read stabilities and write enhanced methods were developed. However, all the advancement in the existing SRAM design exhibited very high dynamic power consumption. The existing stacking and sleep power gating methods needed several rest transistors to reduce the leakage power. Also, none of the existing approaches considered the macro SRAM for reducing the leakage power. In addition, all the existing designs did not perform well when they considered for "frequently read" applications. Hence, there is a requirement of an alternative approach to design SRAM circuits in deep-submicron technologies with minimum leakage power.

## 3. PROPOSED MACRO MEMORY CIRCUIT DESIGN

In this paper, the design of SRAM macro cell is modified by introducing a reversible stacked inverter designs and reversible logic in both differential power generation and peripheral circuits. The proposed SRAM Macro design contains memory cell array with reversible row drivers (RRDs) and Reversible column drivers (RCDs), a read/write controlling module, reversible row decoder and reversible column decoder with data controlling module (DCM). These units are joined together to design SRAM macro as illustrated in Figure 1. Here, the SRAM cell array is designed using 4x4 SRAM cell. The smaller module of SRAM macro design is SRAM cell that stores a single bit value (i.e., "0" or "1"). Here, the control module is used to read the inputs of each array cell, determine the exact operating mode and generate suitable control signals for reading and writing operations. The proposed macro design also introduces a read burst operating (RBO) mode for reducing the read power by experiencing a

read operation in the entire row while RWL (read word line) is stated. It enables the read data to store in reversible latches. As a result of this, a single read operation is sufficient when there is a need of repeated reads on the same row. It reduces the total read power because the reading from the latches consume lesser power than that of the normal read operation. Furthermore, the flow of data in the SRAM cell array is managed by the DCM unit. The Reversible TG based row decoder is used to detect the row in the SRAM cell array at which the address is existing and feeds it to the reversible TG based column decoder for decoding the respective column. In this way, the accurate position of the address can be detected for performing the read or write operation. The RRDs and RCDs are utilized for setting the data on the wordline (WLs) and bitlines (BLs) respectively. In addition, the proposed design utilizes a naïve output buffer for reading the value on RBL (Read BL), which reduces the problems of general-purpose sense amplifier while functioning at sub-threshold voltages.

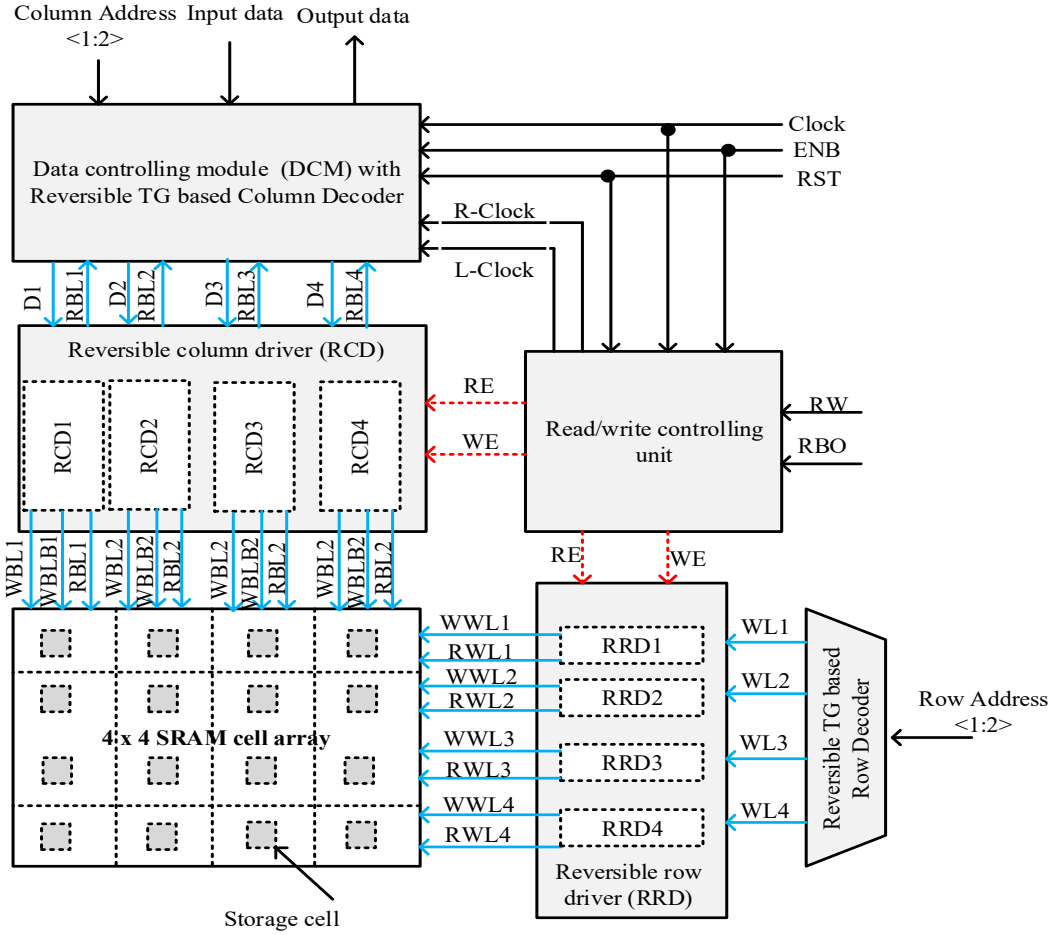



**Fig. 1.** Block diagram of the proposed macro memory design

### *3.1. SRAM cell*

The design of SRAM cell contains two cross-coupled inverters. Here, reversible cross coupled stacked inverter is introduced to minimize the leakage power and ground bouncing noise. The SRAM cell design must consume less power feasibly. Also, the arbitrary circuit of SRAM design should not dissipate the power and therefore, they should be constructed using reversible gate. Hence, an attempt is made to introduce reversible logic in the peripheral circuits of SRAM memory. First, a reversible cross coupled stacked inverter with Transmission gate is adopted in SRAM cell to reduce the leakage power. The PMOS transistors (P1, P2) and NMOS transistors (N1, N2) forms a reversible stacked inverter design. Furthermore, a transmission gates T1 is kept in the inverter design for avoiding the

generation of spurious feedback signals between two conflicting outputs. Here, WE/WEB is set to GND/VDD for keeping the T1in ON state, which preserve the cell stability and protect the saved data via feedback path. Here, the stacking method is introduced by considering the statistic that when more than one transistor is turned OFF in the supply to ground path there is less leakage as compared to single transistor is in OFF state. If input "0" is given to the inverter design, the NMOS transistors are directed to ON condition while the PMOS transistor is directed to OFF condition. Hence, it decreases the leakage current passing through the stacked NMOS transistor by increasing the source to substrate voltage at the upper NMOS transistor and by increasing the drain to source voltage at the lowest NMOS transistor. Implementation of reversible stacked inverter technique with transmission gate leads to low leakage power.

In addition, word line includes two access transistors (N5, N6) for performing peruse and compose activities. The read-decoupled methodology uses access buffers made up of 2 NMOS transistors (N7, N8) to improve read stability. Here, the read current path is decoupled from the storage node for removing the read-disturbances, evading read reverse bias current and improving the RSNM. Furthermore, the writing process of the SRAM is enhanced by introducing reversible logic based differential power generation approach. Figure 2 shows the proposed SRAM cell with assistant circuitry. In this Figure, the write WL (WWL) activates the SRAM cell in row direction and the write bitline pairs (WBL and WBLB) activates the SRAM cell in column direction.

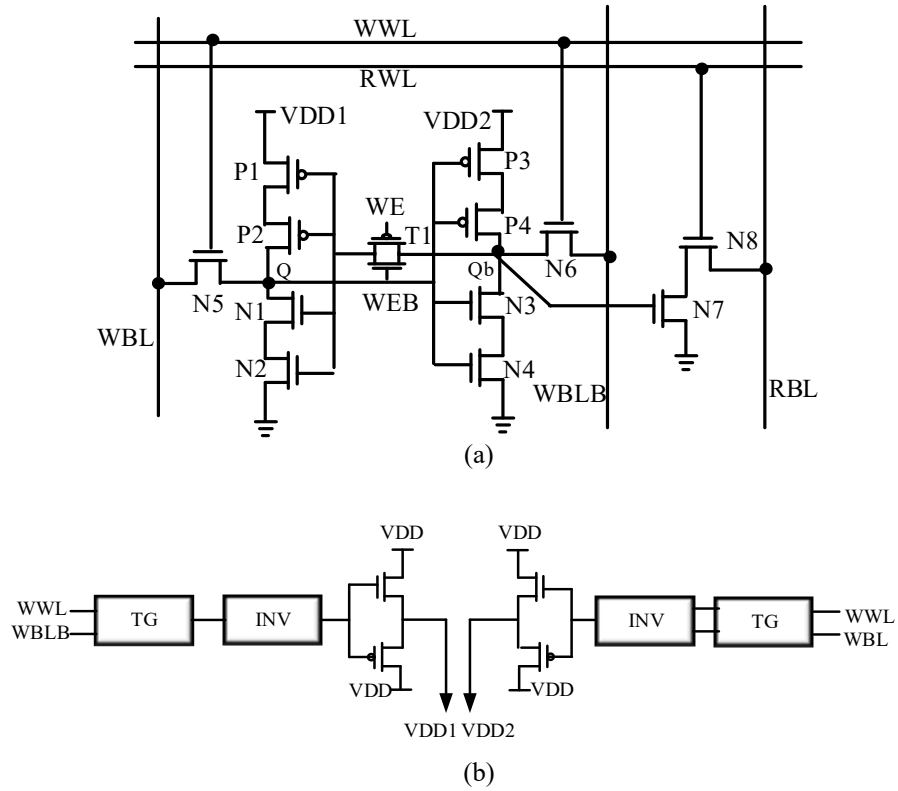



**Fig. 2.** Proposed SRAM design (a) cell circuitry (b) Reversible differential power generation circuitry

Second, a Reversible differential power generation circuitry is used for eliminating the half-selection issue. In general, the write operation is degraded as a result of the half-selection issue. In Figure 2 (a), two distinct power supplies (VDD1 and VDD2) that are generated by the reversible logic based differential power generation approach are connected to the SRAM cell. Here, reversible Toffoli gate is used to obtain VDDM1 that combines WWL and WBLB for driving an inverter to turned ON. Here, the pMOS and nMOS transistor's source terminals are linked to VDD. Likewise, VDDM2 is obtained by

combining CWL and WBL through toffoli gate for driving the power of second inverter to turned ON.

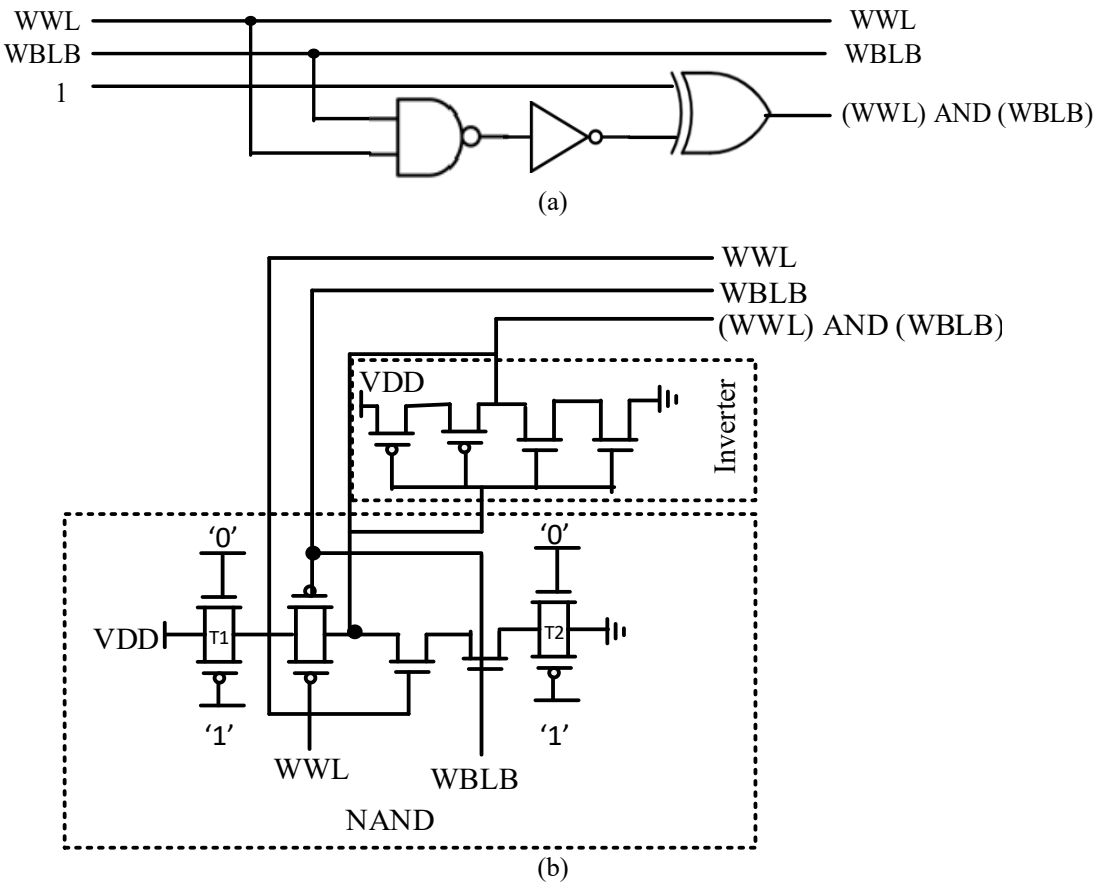



**Fig. 3.** Toffoli gate design (a) Conventional design in CMOS technology (b) Based on SCRL method with standard power supply

One of the modest and familiar universal reversible gates is Toffoli gate. Here, the Split-level Charge Recovery Logic (SCRL) and reversible inverter gates are used to implement Toffoli gate for observing energy recycling. This reversible design is compatibly developed in a CMOS technology. The SCRL method usually saves power by recycling the output capacitance thorough the use of two clocks. These clocks are used for charging and discharging the output capacitance consecutively. This idea is utilized in the reversible TG design for saving the power. The TG gate design using SCRL method is illustrated in Figure 3. WBL and WBLB are inputs and it provides AND output at its third output line. Here, the transmission gates are controlled by the third input of Toffoli gate and its inverse (i.e., 0). In Figure 3 (b), the standard SCRL charge recycling theory is utilized in a different format since two different components such as a NAND gate and NOT gate are used to invent a new Toffoli gate design.

The SCRL NAND gate contains two additional transmission gates $T_1$ and $T_2$. Initially, $T_1$ and $T_2$ are open to enable *Vdd* as the source for charging the complete circuit. The gate is usually transmitting the signal when the transmission gate is in open condition. At the closed condition, it will not transmit any signal. In the subsequent stage, $T_1$ and $T_2$ are switched off. In this condition, the residual energy saved in the wires between the $T_1$ and $T_2$ is imposed the earlier output produced by the NAND into the SCRL NOT for generating a conflicting logic value. This is the reason for lower power consumption of SCRL method as compared to the conventional CMOS Toffoli gate (Figure 3 (a)). Table 1 reports the various signals employed during different operations of the proposed SRAM cell.

**Table 1.** Applied signals during various operations of SRAM cell

| Signal | Write '1' | Write '0' | Read | Hold |
|---|---|---|---|---|
| WBL | 1 | 0 | 0 | 0 |
| WBLB | 0 | 1 | 1 | 0 |
| WE | 1 | 1 | 0 | 0 |
| WEB | 0 | 0 | 1 | 1 |
| WWL | 1 | 1 | 0 | 0 |
| RWL | 0 | 0 | 1 | 0 |

*3.1.1. Write operation*

In the proposed design, the differential VDDs (VDD1 and VDD2) are dropping differentially based on the estimates of the needed write data. The dropping of VDD1 indicates that the data "0" is accessed on WBL (WBLB = 1). At the same time, VDD2 is dropping in reverse direction for accessing write "1". At the time of write operation, the write enable signal WE/WEB is set to VDD/GND for deactivating the T1, which upset the recognized feedback path among the inverter designs. In write "0" operation, the bitline WBL is turned to "0" (WBLB=1) and wordline WWL is turned to "1". Thus, the nMOS transistor placed at the left side of the reversible differential power generation circuitry is turned ON (because WWL and WBLB=1). As a result of this, the voltage is dropping on VDD1, while VDD2 maintains at VDD because the combined result of WWL and WBL is "0". Hence, the pulling up intensity of the PMOS transistors (P1 and P2) are attenuated due to the drooping voltage of VDD1. This allows the access transistor N5 to pull the storage node Q to "0". Likewise, the write "1" operation allows WBL to turned ON and WBLB to drop to "0". Hence, the voltage is dropping on VDD2 (WWL=WBL=1) and the pulling up intensity of PMOS transistors (P3 and P4) are ensured that the node Qb is discharging to zero by the use of N6. The proposed reversible logic based differential power generation approach provides outstanding and valuable influence on the write ability to facilitate the write operation by consuming less power.

*3.1.2. Hold and read operation*

During the hold mode, the access transistors (N5 and N6) are turned OFF due to the lower values on WWL, WBL and WBLB. Hence, the proposed two reversible stacked cross-coupled inverters latch the data. During the read mode, RBL is first pre-charging to the VDD and the higher value of RWL (RWL=1) directs the transistor N8 to turned ON. It activates the read deciding transistor N7 when the node Qb saves "1" and it discharges the RBL to GND via N7 and N8. Alternatively, RBL upholds its pre-charging power when the node Qb saves "0". during the hold and read mode, the signals WE/WEB is set to GND/VDD for ensuring the feedback path between the two reversible stacked cross-coupled inverters by maintaining the transistor T1 in ON stage.

### *3.2. Control and data controlling modules*

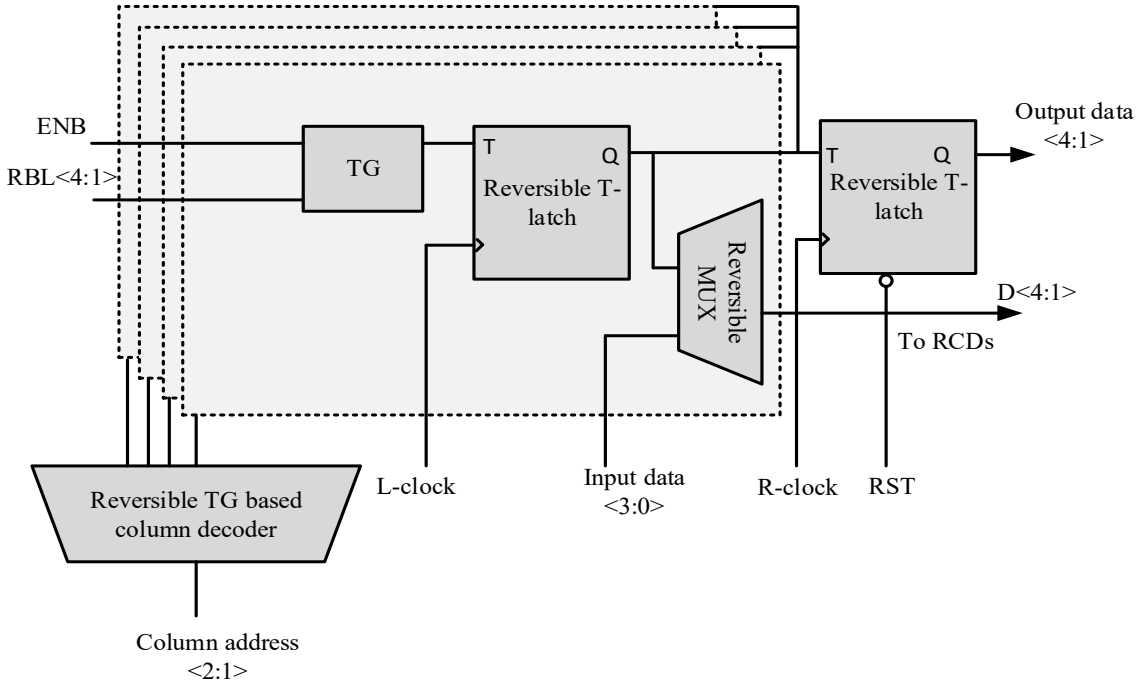
The control unit reads input to each memory cell, determines the exact operating mode, and generates suitable read, write, and control signals. The inputs of controlling unit are ENB, RBO and read/write (RW) and its outputs are read enable (RE), write enable (WE), clock signals (L-clock for latch and R-clock for output buffer). When ENB=1, the controlling module is prompted for reading/writing data into the cell structure. If RW=1, it performs read operation to output the data from the memory cell. Hence, the controlling unit directs RE to turned to "1" and maintain "0" on WE signal. Hence, RE directs the RRDs for setting RWLs. After completing the read operation, the signal L-clock is driven to high for enabling the reversible latches in the DMU to store the data. At last, the controlling unit generates R-clock signal for enabling the output register to output the data. Here, the reversible latches are designed using Peres gate and the Peres gate design utilizes majority gates (MG). The

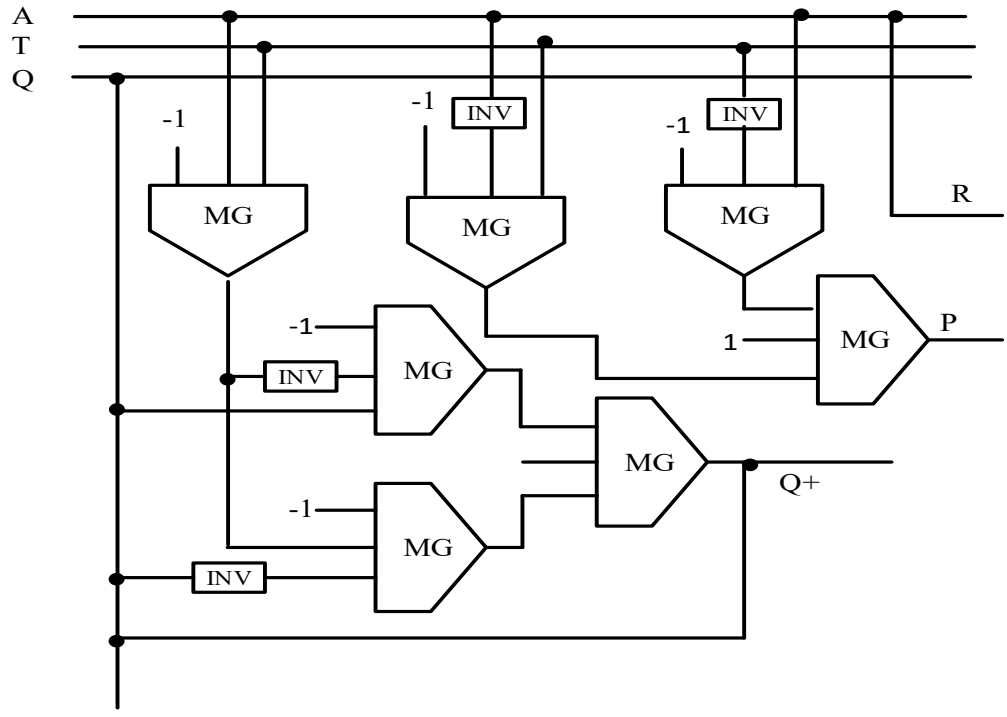
reversible T latch design using MG based Peres gate is shown in Figure 4 (b). When A="0", the data saved in the loop will not be changed and hence the input is ineffective. But the input data is directed towards the loop when the A signal is set to "1". The reversible T latch design can be characterized using the following expression:

$$Q+ = AT \otimes Q \tag{1}$$

The above equation is developed using a single Peres gate. Table 2 provides the truth table of the reversible T latch. These latches are utilized for holding the read information to be utilized while RBO is activated. The detailed diagram of DCM is illustrated in Figure 4 (a).




(a)




(b)

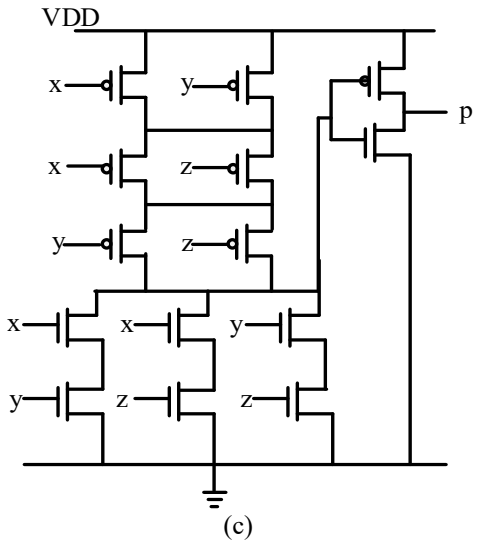



**Fig. 4.** Data controlling module (a) Schematic of DCM (b) Reversible T-latch using peres gate with MG gate implementation (c) Majority gate design

**Table 2.** Truth table for the reversible T latch

| Input | | | Output |
|---|---|---|---|
| ***A*** | ***T*** | ***Q*** | $Q+ = AT \otimes Q$ |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

When the signal RW=0, it performs write operation by enabling WE signal. Hence, WE directs the RRDs and RCDs for setting WWL and WBL/WBLB. In addition, the active input of RBO enables the burst control module placed within the read/write controlling module to save the accessing addresses. If two successive addresses of the same row have been read then the controlling module intimate that the entire data of the respective row is already saved in the latches. As a result of this, the signals RE and and L-clock aren't activated. The DCM block receives RBL, input data, L-clock, R-clock and column addresses to show the output data via register during read operation and gives the input data to the write drivers during write operation.

### *3.3. Reversible row decoder and driver circuits*

In general, the SRAM cell array is formed by arranging the cells in rows and columns. The reversible row and column decoders are mainly used to choose the suitable row and column based on the address bits. The proposed macro memory design uses 2×4 reversible ROW decoder which receives 2-bit address to drive four reversible Toffoli gates (TGs) and activates one of the WLs. Likewise, the reversible column decoder activates different BLs. However, the design of reversible row/column decoders must be adapted to activate one of the RW L or WWL at any interval. To do this, all outputs of the row decoders are connected with 1-to-2 reversible Toffoli gate based demultiplexer. The similar design has been used in the column decoder design. Hence, the RWL and WWL needs different drivers as illustrated in Figure 5.

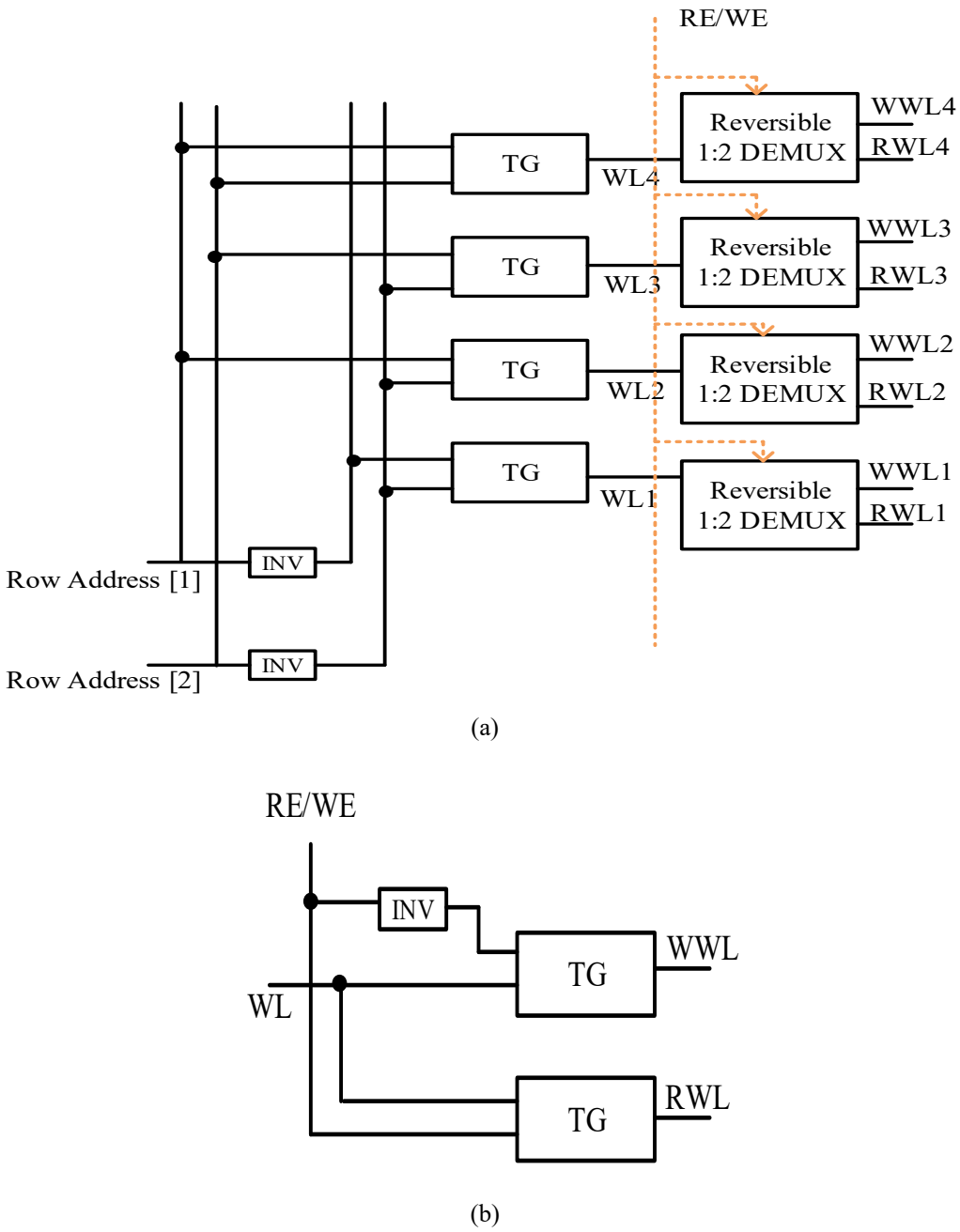



**Fig. 5.** Block diagram of Row decoder (a) Reversible TG based Row decoder (b) Reversible 1:2 DEMUX

It should be noted that the cell structure must write valid data at its storage node for reading exact data (i.e., "0" or "1"). Hence, a write driver is needed to enable exact writing of data. Every writing process begins with pre-charge circuit for pre-charging the bit-lines (i.e., WBL and WBLB). Later, one of the bit-lines is forced to "0" using write driver. At the same time, other bit-line maintains its pre-charged value. If the line WWL is high, the written values are pointed on WBL and WBLB lines. The pre-charge circuit is designed by connecting 3 PMOS transistors on the bit lines (i.e., WBL and WBLB). These bit lines have been connected to the cell. The write driver circuitry is designed by the use of 2 pass transistors (NMOS) transistors and 2 two reversible inverter circuitries. The pass transistors are acting as a transfer component of the SRAM cell, that forces a logic "0" efficiently rather than "1". The write process is executed by writing a "0" into either WBL or WBLB.

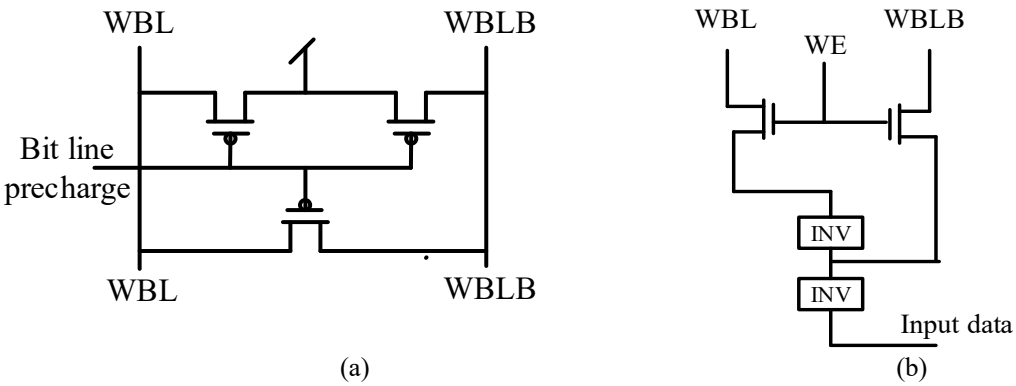



**Fig. 6.** Implementation block for (a) Pre-charge circuit (b) write driver circuit

## 4. SIMULATION RESULTS

Here, the effectiveness of the proposed macro memory design is verified through simulations. The proposed macro memory unit has been simulated in a standard 14 *n*m CMOS process. The SRAM array consists of 4 rows and 4 columns. Every column contains self-supporting differential power rails including VDD1 and VDD2. The area of the proposed cell is slightly larger when compared to recently proposed read and write enhanced SRAM cell. However, the total macro area of a SRAM is smaller due to its simple peripheral circuits. The timing diagrams of write, hold and read operation of the proposed SRAM cell is shown in Figure 7.

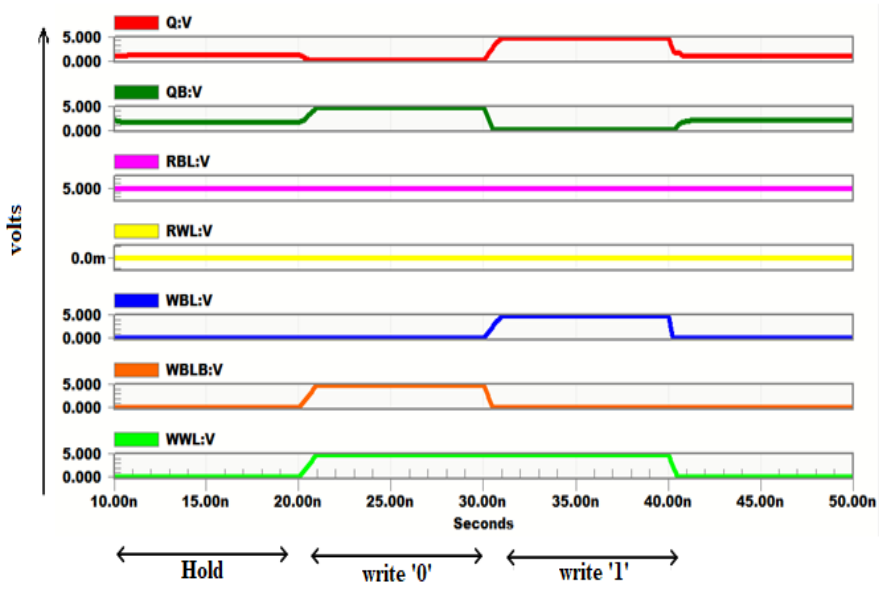



**Fig. 7.** Timing diagrams of hold, write '1' and write '0' operation of the proposed SRAM cell

### *4.1. Static noise margin analysis*

The stability of the SRAM design can be analysed using the measure of Static Noise Margin. Here, the conventional static method (i.e., butterfly method) is introduced to measure the static noise margin (SNM). This SNM can be categorized as Hold Static Noise Margin (HSNM), Read Static Noise Margin (RSNM) and Write Noise Margin (WSNM) based on the mode of operation of SRAM cell. In this section, the SNM analysis of the proposed stacked SRAM design is compared with conventional SRAM design. The WSNM can be determined by embedding a smallest square between the Read and Write voltage transfer characteristics (VTC) as shown in Figure 8 (a). In WSNM measurement, the bit lines (WBL

and WBLB) are pre-charging to VDD and set WWL to "1". This biasing condition yields High voltage at node (Q) while the read VTC curve can be obtained from node Qb. The write VTC can be obtained by pre-charging bitlines WBL to VDD and by connecting WBLB to GND. In this condition, the write VTC is measured. The proposed SRAM design provides WSNM of 250 mV and it is two times higher as compared to conventional SRAM at the supply voltage of 0.6 V. This proves the dominance of the proposed design during write condition. The proposed reversible differential power generator exercises a noticeable beneficial impact on the write ability, easing the write processes.

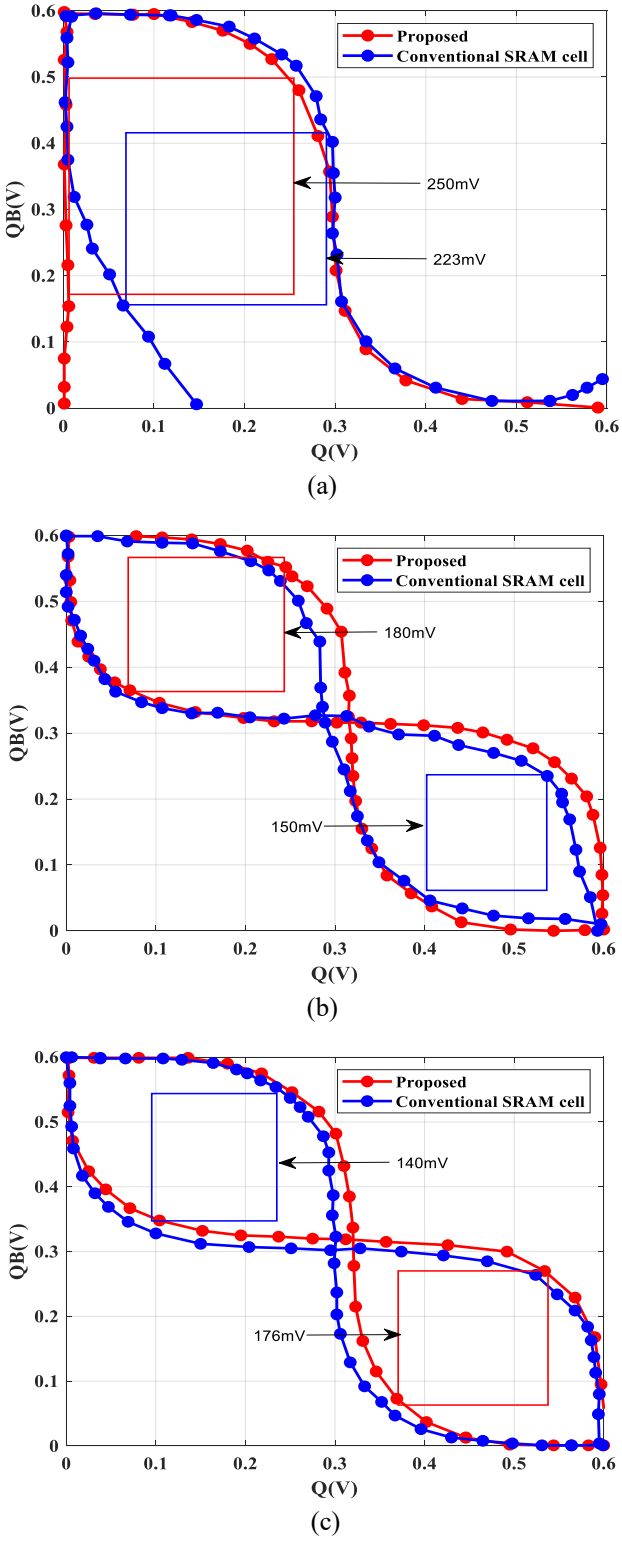



**Fig. 8.** Static noise margin analysis (a) WSNM (b) HSNM (c) RSNM

Fig. 8 (b) illustrates the HSNM of the proposed cell based on butterfly curves at the supply voltage of 0.6 V. This HSNM is computed by inserting a maximum nested square into the butterfly curve. The HSNM of the proposed circuit is increased to 180 mV that is much better than that of the conventional SRAM design. During hold condition, the proposed model does not generate a reverse bias current due to the usage of outward access transistors. Here, the reverse bias current has been eliminated by connecting the access transistors N5 and N6 to ground (since, WBL=WBLB="0"). Furthermore, the stability of the proposed design has also been maintained by keeping the transistor T1 in ON state, which preserved the data saved at storage nodes via feedback path. In RSNM measurement, the RBL is pre-charging to VDD and RWL is set to "1". This biasing condition enable the voltage at node Q to turned VDD from "0". Then, the data is exerted from the tanner tool and drawn a voltage transfer curve of Qb vs. Q as illustrated in Figure 8 (c). Due to the usage of read decoupling method, the storage nodes are isolated from the bit lines that evades the participations of capacitive noise. As a result of this the read upsets have been eliminated by exhibiting a peak RSNM.

### *4.2. Power analysis*

In this section the active power consumption of the proposed macro memory design is analysed in terms of leakage power. The leakage power is also termed as static power and the transistors that aren't fully turned OFF increases the leakage power. Here, the initial analysis is carried out by comparing the proposed reversible transistor stacked SRAM cell design with the existing cell designs to prove its efficiency in leakage power reduction. Table 3 provides the summary of the leakage power of different SRAM cell. The leakage power of the proposed SRAM cell is much better than that of the existing cell designs including 12T SRAM, SE-SRAM and SBL-11T cell design due to the presence of transistor stacking and transmission gate in discharging trail of the proposed cell design during standby mode. Also, the proposed SRAM avoids the reverse bias current due to the usage of outward access transistors. The leakage power of the proposed stacked and reversible logic-based SRAM cell has also been compared with different leakage reduction methodologies to prove its effectiveness in Table 4. The results of this Table shows that the proposed SRAM cell with reversible transistor stacking inverter design with transmission gate consumes only $1.35x10^{-9}$ power. It minimizes the leakage power as compared to the sleep transistor, Sleep and stack, Sleep keeper, Dual stack and DCS respectively.

**Table 3.** Leakage power analysis of different SRAM cell

| SRAM cell | Leakage power (W) | | | |
|---|---|---|---|---|
| | 0.3 | 0.4 | 0.5 | 0.6 |
| 12T SRAM [33] | $0.10x10^{-6}$ | $0.15x10^{-6}$ | $0.20x10^{-6}$ | $0.25x10^{-6}$ |
| SE-SRAM [28] | $1.20x10^{-9}$ | $2.20x10^{-9}$ | $3.30x10^{-9}$ | $5.40x10^{-9}$ |
| SBL-11T [31] | $5.90x10^{-6}$ | $6.40x10^{-6}$ | $7.10x10^{-6}$ | $8.30x10^{-6}$ |
| Proposed | $1.18x10^{-9}$ | $1.24x10^{-9}$ | $1.16x10^{-9}$ | $1.35x10^{-9}$ |

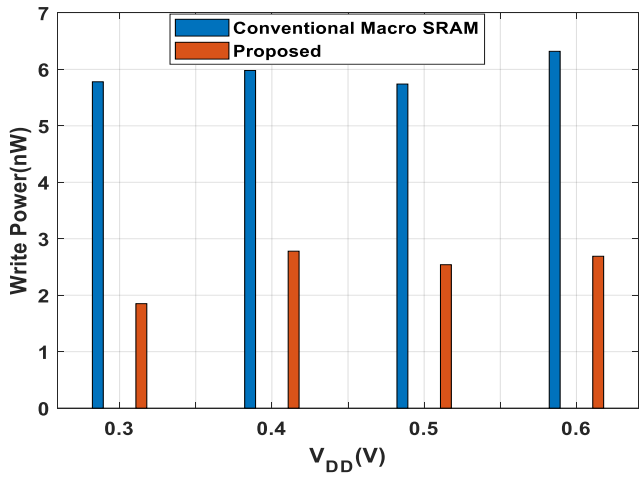
**Table 4.** Leakage power analysis of SRAM cell with different reduction methods

| Method | Leakage power (W) | Method | Leakage power (W) |
|---|---|---|---|
| Sleep transistor | $5.30x10^{-2}$ | Dual stack | $7.00x10^{-2}$ |
| Sleep and stack | $3.40x10^{-2}$ | DCS | $1.80x10^{-2}$ |
| Sleep keeper | $4.90x10^{-2}$ | Proposed Method | $1.35x10^{-9}$ |

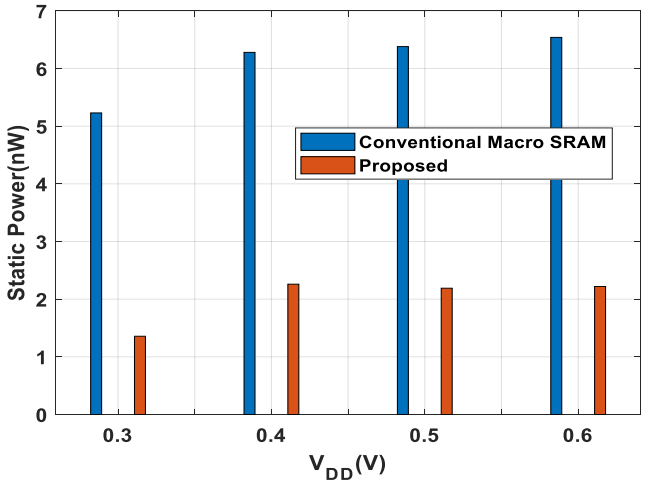
Second, the analysis is carried out by comparing the proposed macro SRAM design with the conventional design in terms of read power, write power and static power. Note that, the

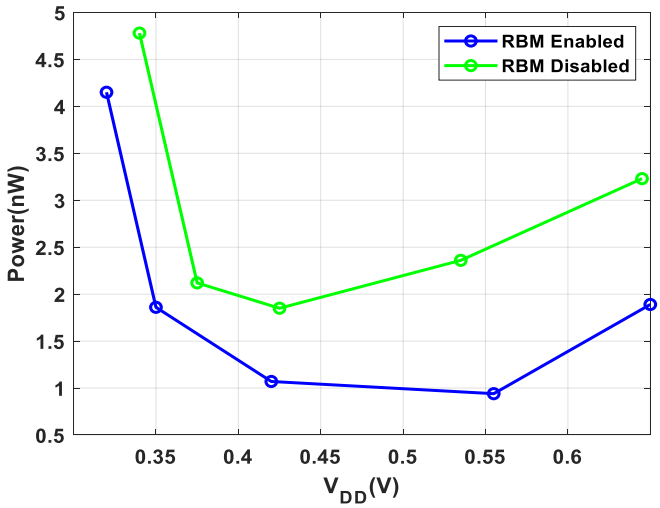
conventional macro design is designed with 8T SRAM cells and irreversible logic based peripheral designs. Due to the introduction of reversible differential power generator in the write assist circuitry, the write power consumption of the proposed macro SRAM is significantly reduced compared with that of the conventional one. Figure 9(a) shows that the write power of the proposed macro memory design is decreased by 57% as compared to conventional macro design at the supply voltage of 0.6 V. It demonstrates the assurance of the proposed macro SRAM for the upcoming memory-dominating low-power applications.




(a)




(b)




(c)

**Fig. 9.** Power analysis of macro memory design (a) write power (b) static power (c) read power

The static power consumption of the proposed macro SRAM design is compared with the conventional macro design in Fig. 9(b). The leakage power of the proposed macro memory design is 66% lesser as compared to the conventional design at the supply voltage of 0.6 V. Because, the proposed SRAM cell don't produce reverse bias current during hold operation due to the introduction of transistor stacking, transmission gate and outward access transistor in the discharge path. Also, most of the peripheral circuits of the macro SRAM design is designed using Toffoli gate with SCRL logic. The energy reversibility property of this logic further used to reduce the power consumption in the proposed macro design. Similarly, the read power consumption of the proposed macro SRAM design is decreased as compared to the conventional macro design. The proposed design also employed a read burst operating mode (RBMO) feature to reduce the read power when consecutive addresses in the same row should be read. The use of this feature has been proven through the results in Figure 9 (c). The proposed model reduced the read power by performing the read process once and storing the data in reversible laches to support the successive reads. The process of data access from the latch consumes considerably lesser power than that of normal read operation. As a result of this, the overall read energy has been reduced.

## 5. CONCLUSION

In this paper, a new macro memory design is proposed based on transistor stacking and reversible logic for solving the issues caused by the leakage power. The proposed SRAM cell provided the best WSNM as compared to the conventional technique through the adoption of a reversible differential power generation based write assist circuit. As a result of this, it has a lower write power. In addition, a read burst mode has been introduced for reducing the read energy while accessing consecutive addresses and it saved 48% of the active read energy.

The proposed SRAM cell reduces the leakage current for showing an enhanced HSNM performance, which indicates the proposed design as a guaranteeing contestant for ultra-low power applications. The introduction of transistor stacking and reversible logics reduced the power consumption down to $1.35nW$ with 0.6V supply. The proposed macro memory design provided the lesser leakage power of $2.22nW$ for the compete cell array as compared to the conventional macro memory design. This research work on SRAM reliability have mainly focused on the memory cell array and memory's peripheral circuitry such as row and column decoders. However, the degradation of the sense amplifier (SA) and the area footprints of the whole circuits were not analysed. This work only compares the power performances of the designs. The existing sense amplifiers may latch incorrect signal and degrades the output of the SRAM system due to offset voltage. In future, a new power-delay compensation circuitry and an ultra-fast offset compensated sense amplifier will be implemented to speed up the read operation, solve the problem of column (row) half-select and determine a good trade-off between delay, energy, area efficiency and sensing reliability.

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